
High-speed CAN Transceiver with Standby Mode CAN FD Ready

DATASHEET

Features

- Fully ISO 11898-2,-5, SAE J2284 compliant
- CAN FD ready
- Communication speed up to 5Mbit/s
- Low electromagnetic emission (EME) and high electromagnetic immunity (EMI)
- Differential receiver with wide common mode range
- Atmel ATA6560: Silent mode (receive only)
- Remote wake-up capability via CAN bus
- Functional behavior predictable under all supply conditions
- Transceiver disengages from the bus when not powered up
- RXD recessive clamping detection
- High electrostatic discharge (ESD) handling capability on the bus pins
- Bus pins protected against transients in automotive environments
- Transmit data (TXD) dominant time-out function
- Undervoltage detection on VCC and VIO pins
- CANH/CANL short-circuit and overtemperature protected
- Qualified according to AEC-Q100
- Packages: SO8, DFN8 with wettable flanks (Moisture Sensitivity Level 1)

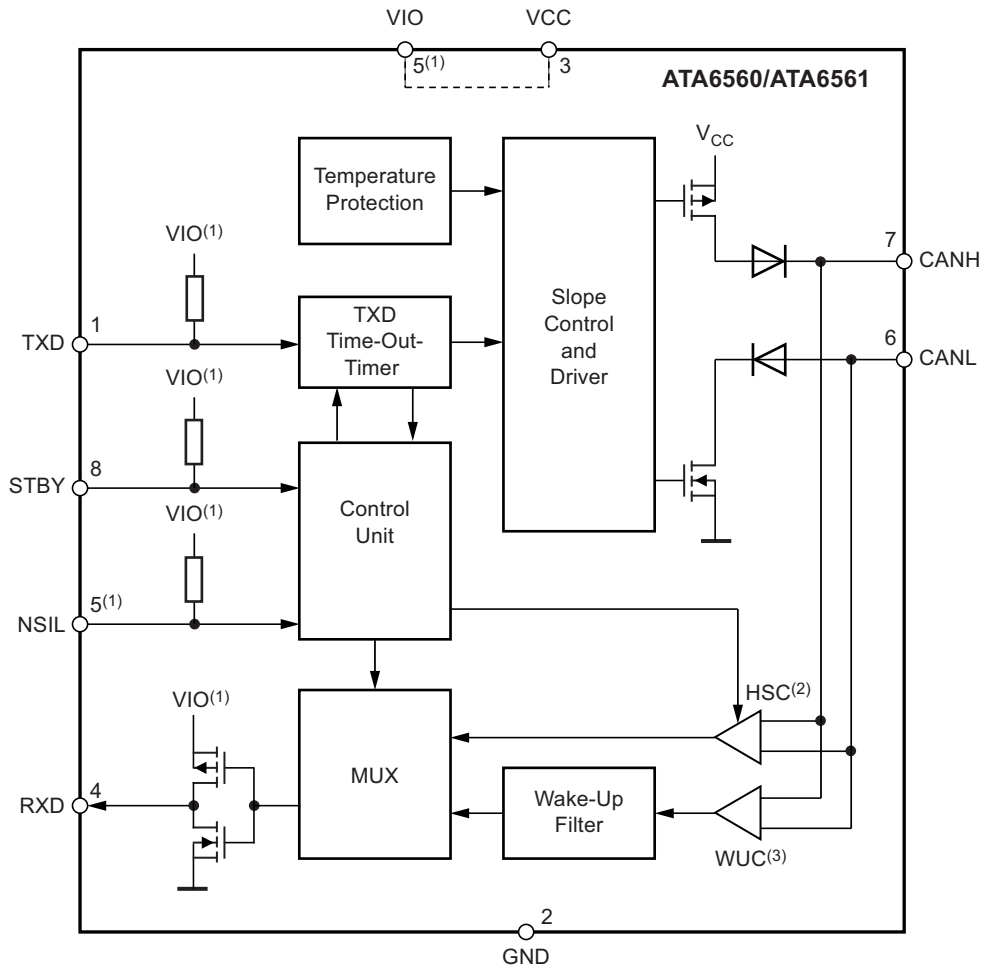
Description

The Atmel® ATA6560/ATA6561 is a high-speed CAN transceiver that provides an interface between a controller area network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed (up to 5Mbit/s) CAN applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller. It offers improved electromagnetic compatibility (EMC) and electrostatic discharge (ESD) performance, as well as features such as:

- Ideal passive behavior to the CAN bus when the supply voltage is off
- Direct interfacing to microcontrollers with supply voltages from 3V to 5V (ATA6561)

Three operating modes together with the dedicated fail-safe features make the Atmel ATA6560/ATA6561 an excellent choice for all types of high-speed CAN networks, especially in nodes requiring low-power mode with wake-up capability via the CAN bus.

Figure 1. Block Diagram



- Notes:
1. Pin 5: Atmel ATA6561: VIO
Atmel ATA6560: NSIL (the VIO line and the VCC line are internally connected)
 2. HSC: High-speed comparator
 3. WUC: Wake-up comparator

1. Pin Configuration

Figure 1-1. SO8 Pinning



Figure 1-2. DFN8 Pinning

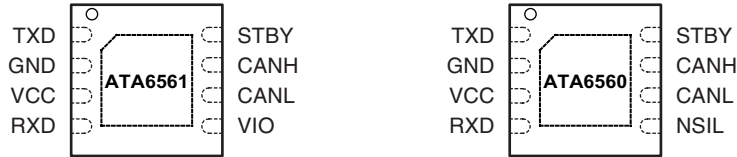


Table 1-1. Pin Description

| Pin | Symbol | Function |
|-------------------------|--------|---|
| 1 | TXD | Transmit data input |
| 2 | GND | Ground supply |
| 3 | VCC | Supply voltage |
| 4 | RXD | Receive data output; reads out data from the bus lines |
| 5 ⁽¹⁾ | VIO | Supply voltage for I/O level adapter; only in the Atmel ATA6561 |
| 5 ⁽¹⁾ | NSIL | Silent mode control input (low active); only in the Atmel ATA6560 |
| 6 | CANL | Low-level CAN bus line |
| 7 | CANH | High-level CAN bus line |
| 8 | STBY | Standby mode control input |
| Backside ⁽²⁾ | - | Heat slug, internally connected to the GND pin |

- Notes:
- The function of pin 5 depends on the version:
Atmel ATA6561: VIO; Atmel ATA6560: NSIL (the VIO line and the VCC line are internally connected)
 - Only for the DFN8 package

2. Functional Description

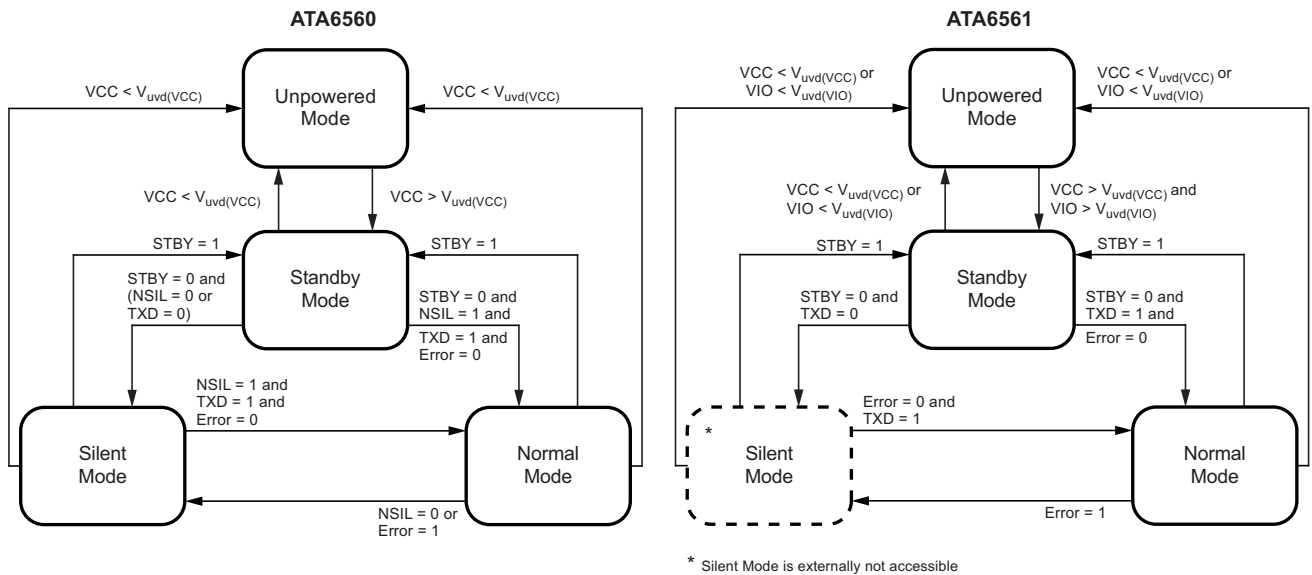
The Atmel® ATA6560/ATA6561 is a stand-alone high-speed CAN transceiver compliant with the ISO 11898-2 and 11898-5 CAN standard. It provides a very low current consumption in standby mode and wake-up capability via the CAN bus. There are two versions available, only differing in the function of pin 5:

- Atmel ATA6561: The pin 5 is the VIO pin and should be connected to the microcontroller supply voltage. This allows direct interfacing to microcontrollers with supply voltages down to 3V and adjusts the signal levels of the TXD, RXD, and STBY pins to the I/O levels of the microcontroller. The I/O ports are supplied by the VIO pin.
- Atmel ATA6560: The pin 5 is the control input for silent mode NSIL allowing the ATA6560 to only receive data but not send data via the bus. The output driver stage is disabled. The VIO line and the VCC line are internally connected, this sets the signal levels of the TXD, RXD, STBY, and NSIL pins to levels compatible with 5V microcontrollers.

2.1 Operating Modes

The Atmel ATA6561 supports three operating modes: unpowered, standby and normal. The Atmel ATA6560 additionally has the silent mode. These modes can be selected via the STBY and NSIL pins. See Figure 2-1 and Table 2-1 for a description of the operating modes.

Figure 2-1. Operating Modes



Note: For the Atmel ATA6561 NSIL is internally set to "1".

Table 2-1. Operating Modes

| Mode | Inputs | | | Outputs | |
|------------------|------------------|---------------------|------------------|------------|-----------------------|
| | STBY | NSIL | Pin TXD | CAN Driver | Pin RXD |
| Unpowered | x ⁽³⁾ | x ⁽³⁾ | x ⁽³⁾ | Recessive | Recessive |
| Standby | HIGH | x ⁽³⁾ | x ⁽³⁾ | Recessive | Active ⁽⁴⁾ |
| Silent (ATA6560) | LOW | LOW | x ⁽³⁾ | Recessive | Active ⁽¹⁾ |
| Normal | LOW | HIGH ⁽²⁾ | LOW | Dominant | LOW |
| | LOW | HIGH ⁽²⁾ | HIGH | Recessive | HIGH |

- Notes:
1. LOW if the CAN bus is dominant, HIGH if the CAN bus is recessive.
 2. Internally pulled up if not bonded out.
 3. Irrelevant
 4. Reflects the bus only for wake-up

2.1.1 Normal Mode

A low level on the STBY pin together with a high level on pins TXD and NSIL selects the normal mode. In this mode the transceiver is able to transmit and receive data via the CANH and CANL bus lines (see [Figure 1 on page 2](#)). The output driver stage is active and drives data from the TXD input to the CAN bus. The high-speed comparator (HSC) converts the analog data on the bus lines into digital data which is output to pin RXD. The bus biasing is set to VCC/2 and the undervoltage monitoring of VCC is active.

The slope of the output signals on the bus lines is controlled and optimized in a way that guarantees the lowest possible electromagnetic emission (EME).

To switch the device in normal operating mode, set the STBY pin to low and the TXD pin and the NSIL pin (if applicable) to high (see [Table 2-1 on page 4](#), [Figure 2-2](#) and [Figure 2-3](#)). The STBY and the NSIL pins each provide a pull-up resistor to VIO, thus ensuring defined levels if the pins are open.

Please note that the device cannot enter Normal Mode as long as TXD is at ground level. Atmel® ATA6560 will only switch to normal mode when all inputs are set accordingly.

The switching into normal mode is depicted in the following two figures.

Figure 2-2. Switching from Standby Mode to Normal Mode (NSIL = High)

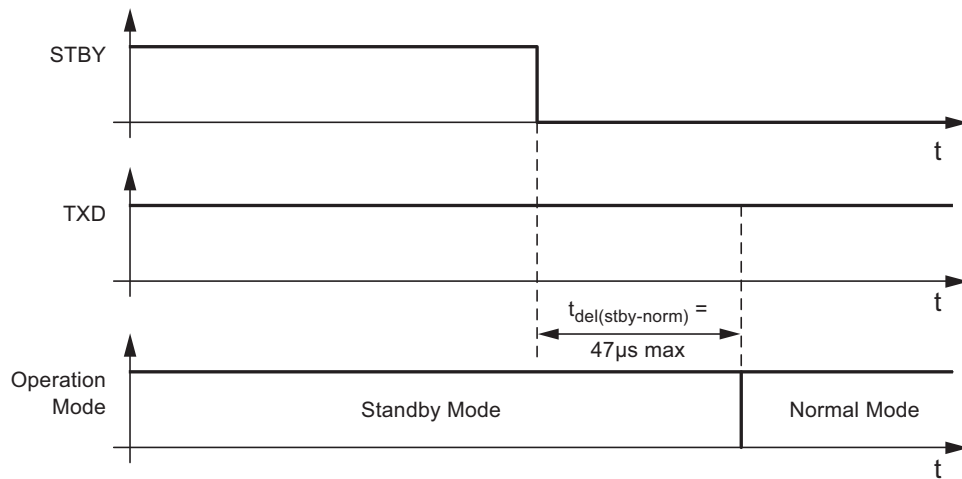
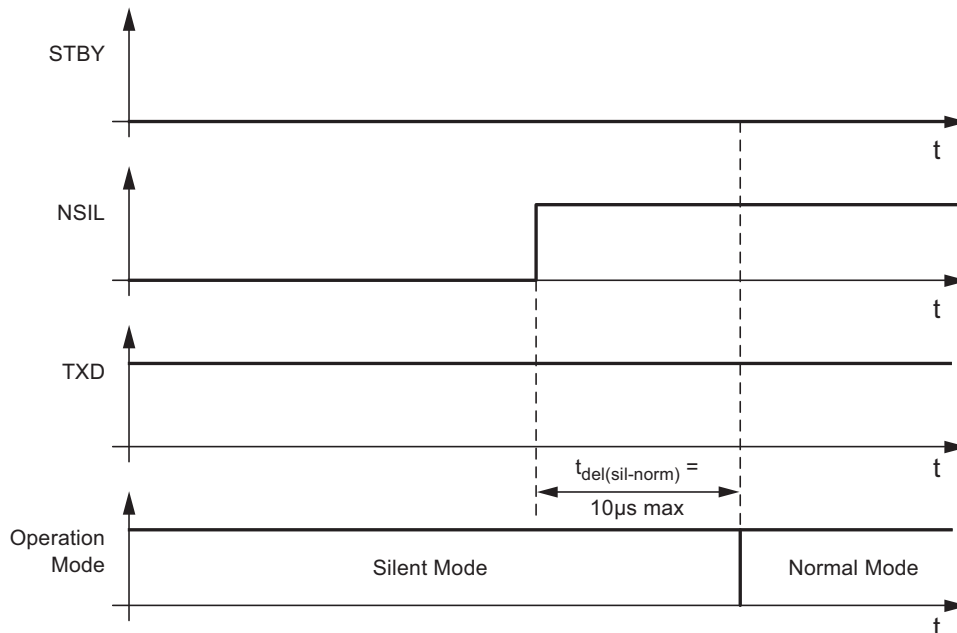


Figure 2-3. Switching from Silent Mode to Normal Mode



2.1.2 Silent Mode (Only with the Atmel ATA6560)

A low level on the NSIL pin (available on pin 5) and on the STBY pin selects silent mode. This receive-only mode can be used to test the connection of the bus medium. In silent mode the Atmel ATA6560 can still receive data from the bus, but the transmitter is disabled and therefore no data can be sent to the CAN bus. The bus pins are released to recessive state. All other IC functions, including the high-speed comparator (HSC), continue to operate as they do in normal mode. Silent mode can be used to prevent a faulty CAN controller from disrupting all network communications.

2.1.3 Standby Mode

A high level on the STBY pin selects standby mode. In this mode the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and the high-speed comparator (HSC) are switched off to reduce current consumption and only the low-power wake-up comparator (WUC) monitors the bus lines for a valid wake-up signal. A signal change on the bus from “Recessive” to “Dominant” followed by a dominant state longer than t_{wake} switches the RXD pin to low to signal a wake-up request to the microcontroller.

In standby mode the bus lines are biased to ground to reduce current consumption to a minimum. The wake-up comparator (WUC) monitors the bus lines for a valid wake-up signal. When the RXD pin switches to low to signal a wake-up request, a transition to normal mode is not triggered until the STBY pin is forced back to low by the microcontroller. A bus dominant time-out timer prevents the device from generating a permanent wake-up request by switching the RXD pin to high.

For Atmel® ATA6560 only: In the event the NSIL input pin is set to low in standby mode, the internal pull-up resistor causes an additional quiescent current from VIO to GND. Atmel therefore recommends setting the NSIL pin to high in standby mode.

2.2 Fail-safe Features

2.2.1 TXD Dominant Time-Out Function

A TXD dominant time-out timer is started when the TXD pin is set to LOW. If the LOW state on the TXD pin persists for longer than $t_{\text{to(dom)TXD}}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when the TXD pin is set to HIGH ($\geq 4\mu\text{s}$).

2.2.2 Internal Pull-Up Structure at the TXD, NSIL, and STBY Input Pins

The TXD, STBY, and NSIL pins have an internal pull-up to VIO. This ensures a safe, defined state in case one or all of these pins are left floating. Pull-up currents flow in these pins in all states, meaning all pins should be in high state during standby mode to minimize the current consumption.

2.2.3 Undervoltage Detection on Pins VCC and VIO

If V_{VCC} or V_{VIO} drop below their respective undervoltage detection levels ($V_{\text{uvd(VCC)}}$ and $V_{\text{uvd(VIO)}}$) (see [Section 6. “Electrical Characteristics” on page 9](#)), the transceiver switches off and disengages from the bus until V_{VCC} and V_{VIO} have recovered. The low-power wake-up comparator is only switched off during a VCC or VIO undervoltage. The logic state of the STBY pin is ignored until the VCC voltage or the VIO voltage has recovered.

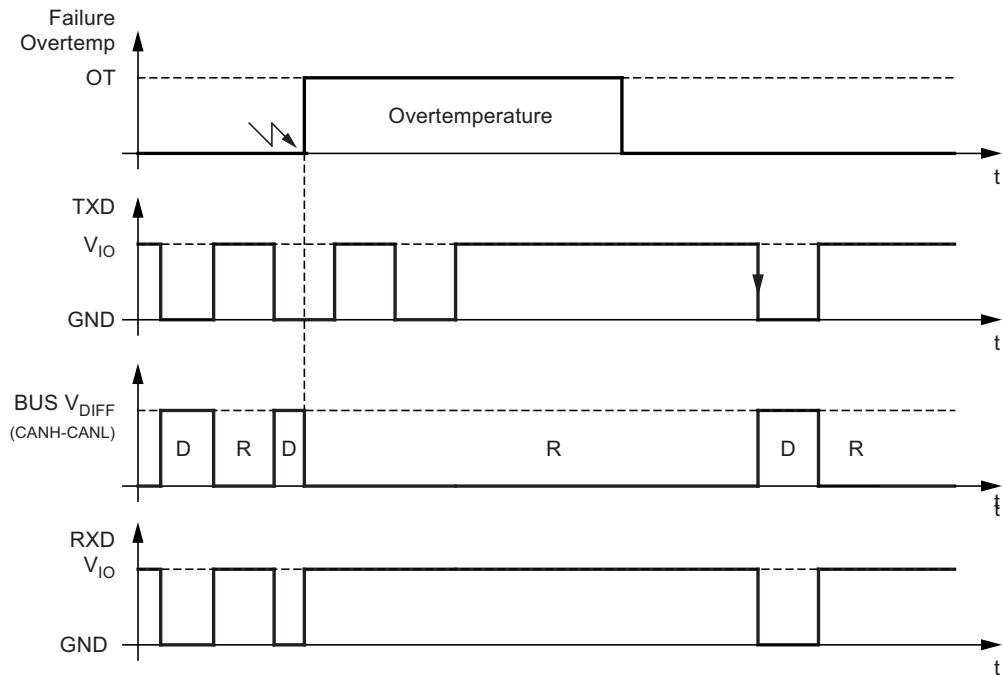
2.2.4 Bus Wake-up Time-out Function

In standby mode a bus wake-up time-out timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than $t_{\text{to_bus}}$, the RXD pin is switched to HIGH. This function prevents a clamped dominant bus (due to a bus short-circuit or a failure in one of the other nodes on the network) from generating a permanent wake-up request. The bus wake-up time-out timer is reset when the CAN bus changes from dominant to recessive state.

2.2.5 Overtemperature Protection

The output drivers are protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature, T_{Jsd} , the output drivers are disabled until the junction temperature drops below T_{Jsd} and pin TXD is at high level again. The TXD condition ensures that output driver oscillations due to temperature drift are avoided.

Figure 2-4. Release of Transmission after Overtemperature Condition



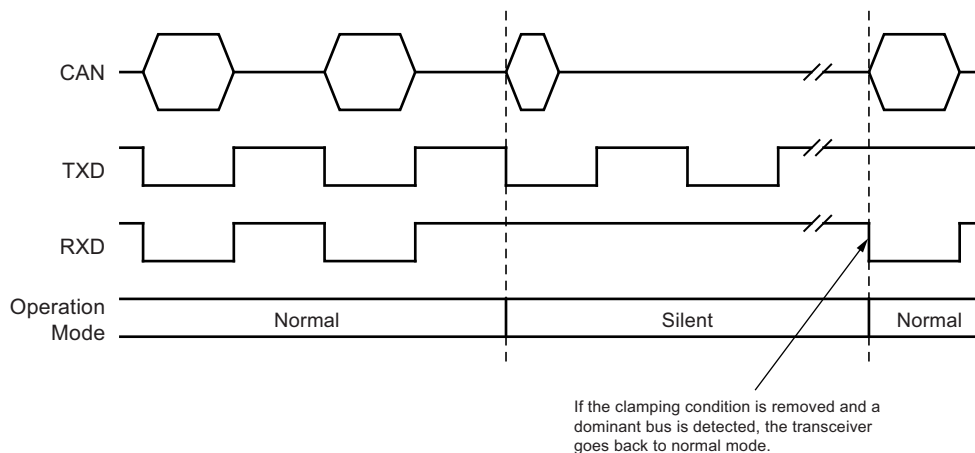
2.2.6 Short-Circuit Protection of the Bus Pins

The CANH and CANL bus outputs are short-circuit protected, either against GND or a positive supply voltage. A current-limiting circuit protects the transceiver against damage. If the device is heating up due to a continuous short on CANH or CANL, the internal overtemperature protection switches the bus transmitter off.

2.2.7 RXD Recessive Clamping

This fail-safe feature prevents the controller from sending data on the bus if its RXD line is clamped to HIGH (e.g., recessive). That is, if the RXD pin cannot signalize a dominant bus condition because it is e.g., shorted to VCC, the transmitter within ATA6560/ATA6561 is disabled to avoid possible data collisions on the bus. In normal and silent mode (only ATA6560), the device permanently compares the state of the high-speed comparator (HSC) with the state of the RXD pin. If the HSC indicates a dominant bus state for more than t_{RC_det} without the RXD pin doing the same, a recessive clamping situation is detected and the device is forced into silent mode. This fail-safe mode is released by either entering standby or unpowered mode or if the RXD pin is showing a dominant (e.g., LOW) level again.

Figure 2-5. RXD Recessive Clamping Detection



3. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Condition | Symbol | Min. | Max. | Unit |
|---|-----------|----------------------|------|------|------|
| CANH, CANL DC voltage Transient voltage, according to ISO 7637 part 2 | | V_{CANH}, V_{CANL} | -27 | +42 | V |
| DC voltage on all other pins | | V_X | -0.3 | +5,5 | V |
| ESD according to IBEE LIN EMC Test spec. 1.0 following IEC 61000-4-2 - Pin CANH, CANL | | | ±8 | | kV |
| ESD (HBM following STM5.1 with 1.5kΩ/100pF) - Pin CANH, CANL to GND | | | ±6 | | kV |
| Component Level ESD (HBM acc. ANSI/ESD STM5.1) JESD22-A114 AEC-Q100 (002) | | | ±4 | | kV |
| CDM ESD STM 5.3.1 | | | ±750 | | V |
| ESD machine model AEC-Q100-RevF(003) | | | ±200 | | V |
| Operating range for junction temperature | | T_j | -40 | +150 | °C |
| Storage temperature | | T_{stg} | -55 | +150 | °C |

4. Thermal Characteristics SO8

| Parameters | Symbol | Min. | Typ. | Max. | Unit |
|--|------------|------|------|------|------|
| Thermal resistance junction to ambient | R_{thJA} | | 145 | | K/W |
| Thermal shutdown of the bus drivers | T_{Jsd} | 150 | 175 | 195 | °C |

5. Thermal Characteristics DFN8

| Parameters | Symbol | Min. | Typ. | Max. | Unit |
|---|------------|------|------|------|------|
| Thermal resistance junction to heat slug | R_{thJC} | | 10 | | K/W |
| Thermal resistance junction to ambient, where heat slug is soldered to PCB according to JEDEC | R_{thJA} | | 50 | | K/W |
| Thermal shutdown of the bus drivers | T_{Jsd} | 150 | 175 | 195 | °C |

6. Electrical Characteristics

$T_j = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; $V_{CC} = 4.5\text{V}$ to 5.5V ; $V_{IO} = 2.8\text{V}$ to 5.5V ; $R_L = 60\Omega$, $C_L = 100\text{pF}$ unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

| No. | Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|--|---|----------------------|------------|----------------------|---|-------------|
| 1 Supply, Pin V_{CC} | | | | | | | | |
| 1.1 | Supply voltage | | V_{CC} | 4.5 | | 5.5 | V | A |
| 1.2 | Supply current in silent mode | Silent mode, $V_{TXD} = V_{VIO}$ | I_{VCC_sil} | 1.9 | 2.5 | 3.0 | mA | A |
| 1.3 | Supply current in normal mode | - recessive, $V_{TXD} = V_{VIO}$ - dominant, $V_{TXD} = 0\text{V}$ | I_{VCC_rec} I_{VCC_dom} | 2 20 | 50 | 5 70 | mA mA | A |
| 1.4 | Supply current in STBY mode | $V_{CC} = V_{IO}$, $V_{TXD} = V_{NSIL} = V_{VIO}$ $T_a = 25^{\circ}\text{C}$ | I_{VCC_STBY} I_{VCC_STBY} | | 7 | 12 | μA μA | A D |
| 1.5 | Undervoltage detection threshold on pin VCC | | $V_{uvd(VCC)}$ | 2.75 | | 4.5 | V | A |
| 2. I/O Level Adapter Supply, Pin VIO⁽¹⁾ (only with the Atmel ATA6561) | | | | | | | | |
| 2.1 | Supply voltage on pin VIO | | V_{VIO} | 2.8 | | 5.5 | V | A |
| 2.2 | Supply current on pin VIO | Normal and silent mode - recessive, $V_{TXD} = V_{VIO}$ - dominant, $V_{TXD} = 0\text{V}$ STBY mode | I_{IO_rec} I_{IO_rdom} I_{IO_STBY} | 10 50 | 80 350 | 250 500 1 | μA μA μA | A A A |
| 2.3 | Undervoltage detection threshold on pin VIO | | $V_{uvd(VIO)}$ | 1.3 | | 2.7 | V | A |
| 3 Mode Control Input, Pin NSIL and STBY | | | | | | | | |
| 3.1 | High-level input voltage | | V_{IH} | $0.7 \times V_{VIO}$ | | $V_{VIO} + 0.3$ | V | A |
| 3.2 | Low-level input voltage | | V_{IL} | -0.3 | | $0.3 \times V_{VIO}$ | V | A |
| 3.3 | Pull-up resistor to VIO | $V_{STBY} = 0\text{V}$ $V_{NSIL} = 0\text{V}$ | R_{pu} | 75 | 125 | 175 | k Ω | A |
| 3.4 | High-level leakage current | $V_{STBY} = V_{VIO}$ $V_{NSIL} = V_{VIO}$ | I_L | -2 | | +2 | μA | A |
| 4 CAN Transmit Data Input, Pin TXD | | | | | | | | |
| 4.1 | High-level input voltage | | V_{IH} | $0.7 \times V_{VIO}$ | | $V_{VIO} + 0.3$ | V | A |
| 4.2 | Low-level input voltage | | V_{IL} | -0.3 | | $0.3 \times V_{VIO}$ | V | A |
| 4.3 | Pull-up resistor to VIO | $V_{TXD} = 0\text{V}$ | R_{TXD} | 20 | 35 | 50 | k Ω | A |
| 4.4 | High-level leakage current | Normal mode, $V_{TXD} = V_{VIO}$ | I_{TXD} | -2 | | +2 | μA | A |
| 4.5 | Input capacitance | | C_{TXD} | | 5 | 10 | pF | D |
| 5 CAN Receive Data Output, Pin RXD | | | | | | | | |
| 5.1 | High-level output current | Normal mode, $V_{RXD} = V_{VIO} - 0.4\text{V}$, $V_{VIO} = V_{VCC}$ | I_{OH} | -8 | | -1 | mA | A |
| 5.2 | Low-level output current | Normal mode, $V_{RXD} = 0.4\text{V}$, bus dominant | I_{OL} | 2 | | 12 | mA | A |
| 6 Bus Lines, Pins CANH and CANL | | | | | | | | |
| 6.1 | Dominant output voltage | $V_{TXD} = 0\text{V}$, $T < t_{to(dom)TXD}$ - pin CANH - pin CANL | I_{IO} | 2.75 0.5 | 3.5 1.5 | 4.5 2.25 | V V | A |
| 6.2 | Transmitter dominant voltage symmetry | $V_{dom(TX)sym} = V_{VCC} - V_{CANH} - V_{CANL}$ | $V_{dom(TX)sym}$ | -400 | | +400 | mV | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Only for Atmel ATA6560; otherwise the values are part of the VCC pin specification.

6. Electrical Characteristics (Continued)

$T_j = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; $V_{CC} = 4.5\text{V}$ to 5.5V ; $V_{IO} = 2.8\text{V}$ to 5.5V ; $R_L = 60\Omega$, $C_L = 100\text{pF}$ unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

| No. | Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|--|--|---------------------|------------|----------------------|------------|------------------|-------|
| 6.3 | Bus differential output voltage | $V_{TXD} = 0\text{V}$, $T < t_{to(dom)TXD}$ $R_L = 45\Omega$ to 65Ω $V_{VCC} = 4.75\text{V}$ to 5.25V $V_{TXD} = V_{VIO}$, receive, no load | $V_{O(dif)bus}$ | 1.5 -50 | | 3 +50 | V mV | A |
| 6.4 | Recessive output voltage | Normal and silent modes, $V_{TXD} = V_{VIO}$, no load | $V_{O(rec)}$ | 2 | $0.5 \times V_{VCC}$ | 3 | V | A |
| 6.5 | Differential receiver threshold voltage (HSC) | Normal and silent modes, $V_{cm(CAN)} = -27\text{V}$ to $+27\text{V}$ | $V_{th(RX)dif}$ | 0.5 | 0.7 | 0.9 | V | A |
| 6.6 | Differential receiver hysteresis voltage (HSC) | Normal and silent modes, $V_{cm(CAN)} = -27\text{V}$ to $+27\text{V}$ | $V_{hys(RX)dif}$ | 50 | 120 | 200 | mV | A |
| 6.7 | Dominant output current | $V_{TXD} = 0\text{V}$, $T < t_{to(dom)TXD}$, $V_{VCC} = 5\text{V}$ - pin CANH, $V_{CANH} = 0\text{V}$ - pin CANL, $V_{CANL} = 5\text{V}/40\text{V}$ | $I_{IO(dom)}$ | -100 35 | | -35 100 | mA mA | A |
| 6.8 | Recessive output current | Normal and silent modes, $V_{TXD} = V_{VIO}$, no load, $V_{CANH} = V_{CANL} = -27\text{V}$ to $+32\text{V}$ | $I_{IO(rec)}$ | -5 | | +5 | mA | A |
| 6.9 | Leakage current | $V_{VCC} = V_{VIO} = 0\text{V}$, $V_{CANH} = V_{CANL} = 5\text{V}$ | $I_{IO(rec)}$ | -5 | 0 | +5 | μA | A |
| 6.10 | Input resistance | | R_i | 9 | 15 | 28 | $\text{k}\Omega$ | A |
| 6.11 | Input resistance deviation | Between V_{CANH} and V_{CANL} | ΔR_i | -1 | 0 | +1 | % | A |
| 6.12 | Differential input resistance | $T_j < 125^{\circ}\text{C}$ | $R_{i(dif)}$ | 19 | 30 | 52 | $\text{k}\Omega$ | A |
| | | | $R_{i(dif)}$ | 20 | 30 | 52 | $\text{k}\Omega$ | B |
| 6.13 | Common-mode input capacitance | | $C_{i(cm)}$ | | | 20 | pF | D |
| 6.14 | Differential input capacitance | | $C_{i(dif)}$ | | | 10 | pF | D |
| 8 Transceiver Timing, Pins CANH, CANL, TXD, and RXD, see Figure 6-1 and Figure 6-2 | | | | | | | | |
| 8.1 | Delay time from TXD to bus dominant | Normal mode | $t_{d(TXD-busdom)}$ | 40 | | 130 | ns | C |
| 8.2 | Delay time from TXD to bus recessive | Normal mode | $t_{d(TXD-busrec)}$ | 40 | | 130 | ns | C |
| 8.3 | Delay time from bus dominant to RXD | Normal and silent modes | $t_{d(busdom-RXD)}$ | 20 | | 100 | ns | C |
| 8.4 | Delay time from bus recessive to RXD | Normal and silent modes | $t_{d(busrec-RXD)}$ | 20 | | 100 | ns | C |
| 8.5 | Propagation delay from TXD to RXD | Normal mode Rising edge at pin TXD Falling edge at pin TXD | $t_{PD(TXD-RXD)}$ | 40 | | 200 | ns | A |
| | | | | 40 | | 200 | ns | A |
| | | Normal mode $R_L = 120\Omega$, $C_L = 200\text{pF}$ Rising edge at pin TXD Falling edge at pin TXD | $t_{PD(TXD-RXD)}$ | | | 300 | ns | D |
| | | | | | | 300 | ns | D |
| 8.6 | TXD dominant time-out time | $V_{TXD} = 0\text{V}$, normal mode | $t_{to(dom)TXD}$ | 0.8 | | 3 | ms | A |
| 8.7 | Bus wake-up time-out time | Standby Mode | t_{to_bus} | 0.8 | | 3 | ms | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Only for Atmel ATA6560; otherwise the values are part of the VCC pin specification.

6. Electrical Characteristics (Continued)

$T_j = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; $V_{CC} = 4.5\text{V}$ to 5.5V ; $V_{IO} = 2.8\text{V}$ to 5.5V ; $R_L = 60\Omega$, $C_L = 100\text{pF}$ unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

| No. | Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit | Type* |
|--|--|--|------------------------------------|------|------|------|---------------|-------|
| 8.8 | Min. dominant time for bus wake-up | Standby mode | t_{wake} | 0.75 | 3 | 5 | μs | A |
| 8.9 | Delay time for standby to normal mode transition | Falling edge at pin STBY NSIL = HIGH | $t_{\text{del}}(\text{stby-norm})$ | | | 47 | μs | A |
| 8.10 | Delay time for normal mode to standby mode transition | Rising edge at pin STBY NSIL = HIGH | $t_{\text{del}}(\text{norm-stby})$ | | | 5 | μs | D |
| 8.11 | Delay time for normal mode to silent mode transition | Falling edge at pin NSIL STBY = LOW | $t_{\text{del}}(\text{norm-sil})$ | | | 10 | μs | D |
| 8.12 | Delay time for silent mode to normal mode transition | Rising edge at pin NSIL STBY = LOW | $t_{\text{del}}(\text{sil-norm})$ | | | 10 | μs | D |
| 8.13 | Delay time for silent mode to standby mode transition | Rising edge at pin STBY NSIL = LOW | $t_{\text{del}}(\text{sil-stby})$ | | | 5 | μs | D |
| 8.14 | Delay time for standby mode to silent mode transition | Falling edge at pin STBY NSIL = LOW | $t_{\text{del}}(\text{stby-sil})$ | | | 47 | μs | D |
| 8.15 | Debouncing time for recessive clamping state detection | $V(\text{CANH-CANL}) > 900\text{mV}$ RXD = HIGH | $t_{\text{RC_det}}$ | | 90 | | ns | D |
| Transceiver Timing for higher Bit Rates, Pins CANH, CANL, TXD, and RXD, see Figure 6-1 and Figure 6-3 on page 12 | | | | | | | | |
| 8.16 | Recessive bit time on pin RXD | Normal mode, $t_{\text{Bit}}(\text{TXD}) = 500\text{ns}$ | $t_{\text{Bit}}(\text{RXD})$ | 400 | | 550 | ns | D |
| | | Normal mode, $t_{\text{Bit}}(\text{TXD}) = 200\text{ns}$ | $t_{\text{Bit}}(\text{RXD})$ | 120 | | 220 | ns | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Only for Atmel ATA6560; otherwise the values are part of the VCC pin specification.

Figure 6-1. Timing Test Circuit for the Atmel ATA6560/ATA6561 CAN Transceiver

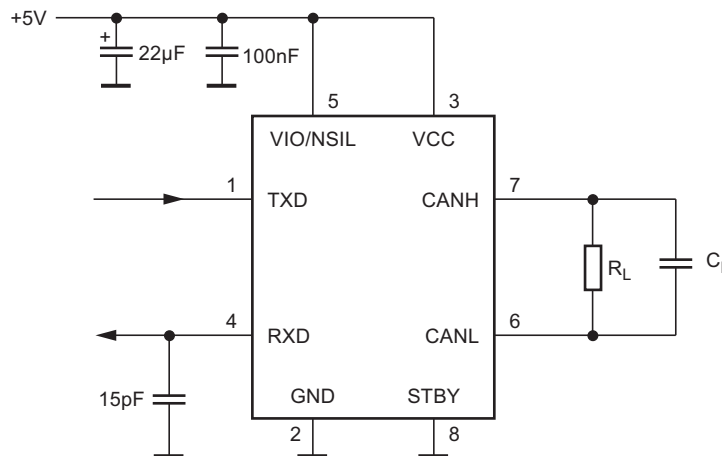


Figure 6-2. CAN Transceiver Timing Diagram

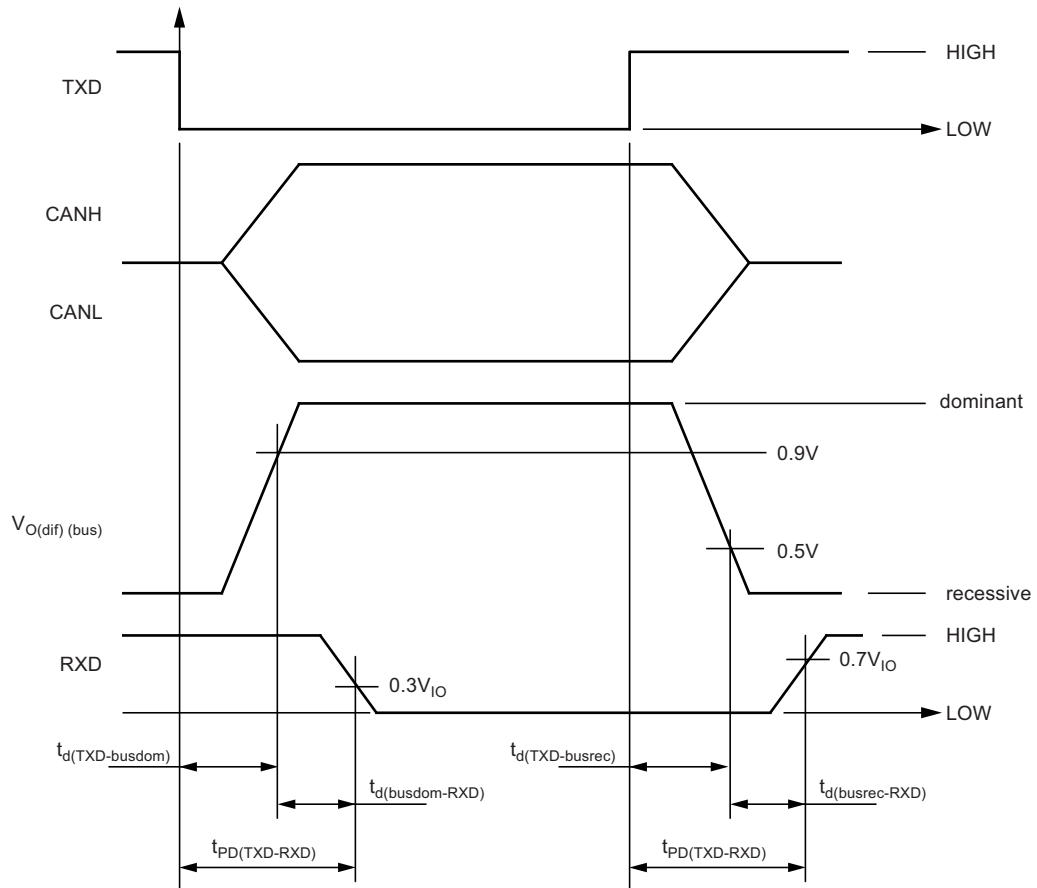
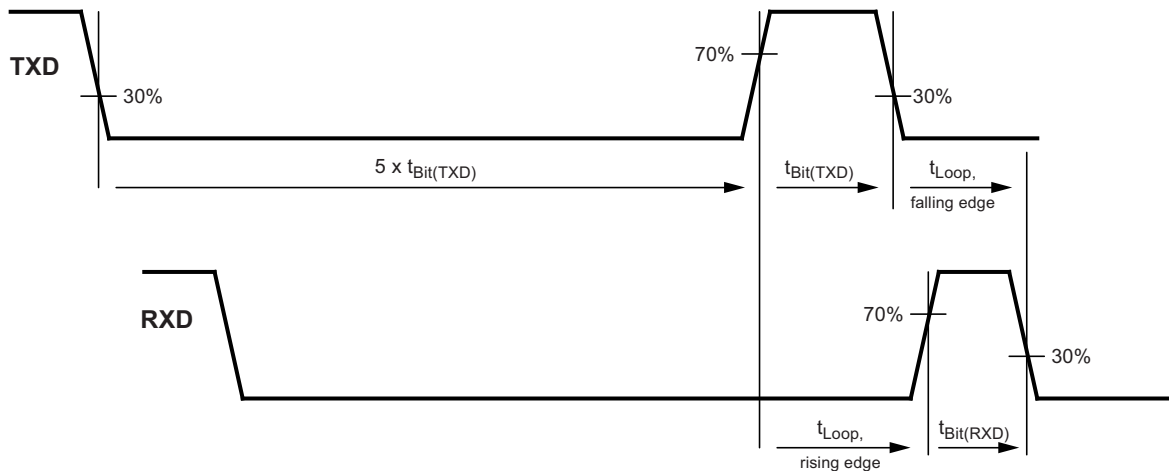


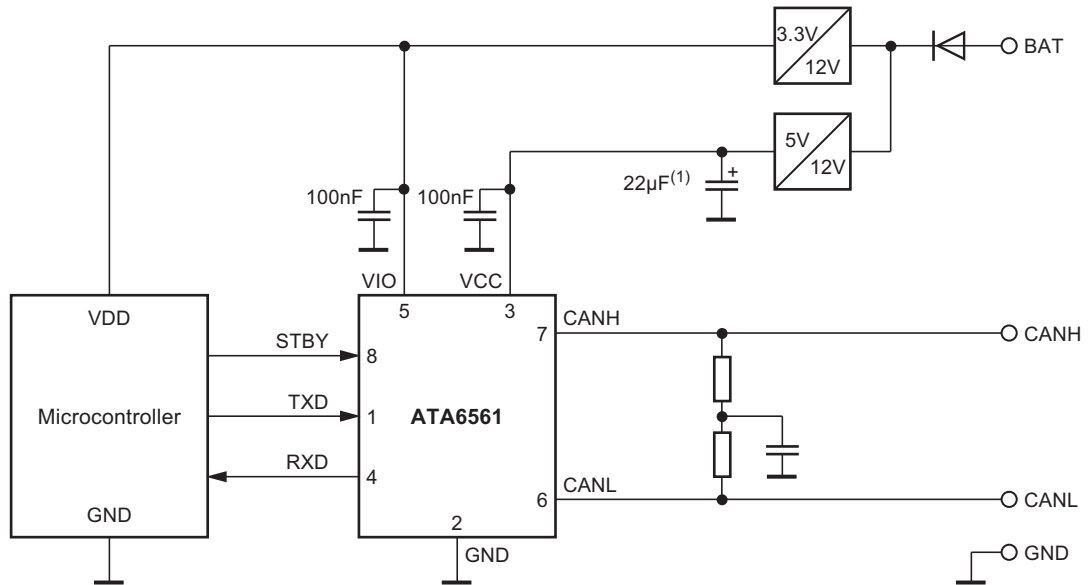
Figure 6-3. Can Transceiver Timing Diagram for Loop Delay Symmetry



Note: The bit time of a recessive bit after five dominant bits is measured on the RXD pin.

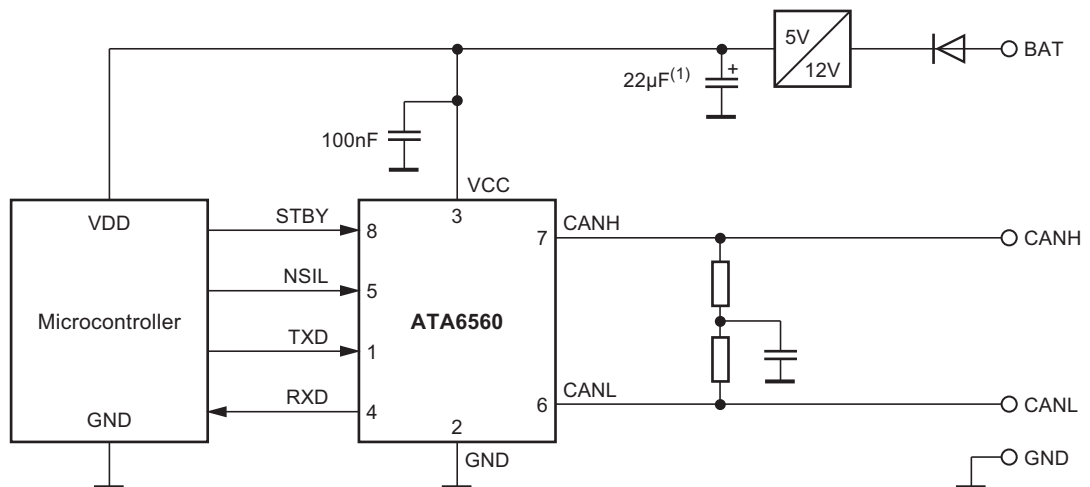
7. Application Circuits

Figure 7-1. Typical Application Circuit Atmel ATA6561



(1) The size of this capacitor depends on the used external voltage regulator.

Figure 7-2. Typical Application Circuit Atmel ATA6560



(1) The size of this capacitor depends on the used external voltage regulator.

Note: For DFN8 package: Heat slug must always be connected to GND.

8. Ordering Information

| Extended Type Number | Package | Remarks |
|----------------------|---------|--|
| ATA6560-GBQW | DFN8 | CAN transceiver, Pb-free, 6k, taped and reeled |
| ATA6560-GAQW | SO8 | CAN transceiver, Pb-free, 4k, taped and reeled |
| ATA6561-GBQW | DFN8 | CAN transceiver, Pb-free, 6k, taped and reeled |
| ATA6561-GAQW | SO8 | CAN transceiver, Pb-free, 4k, taped and reeled |

9. Package Information

Figure 9-1. SO8

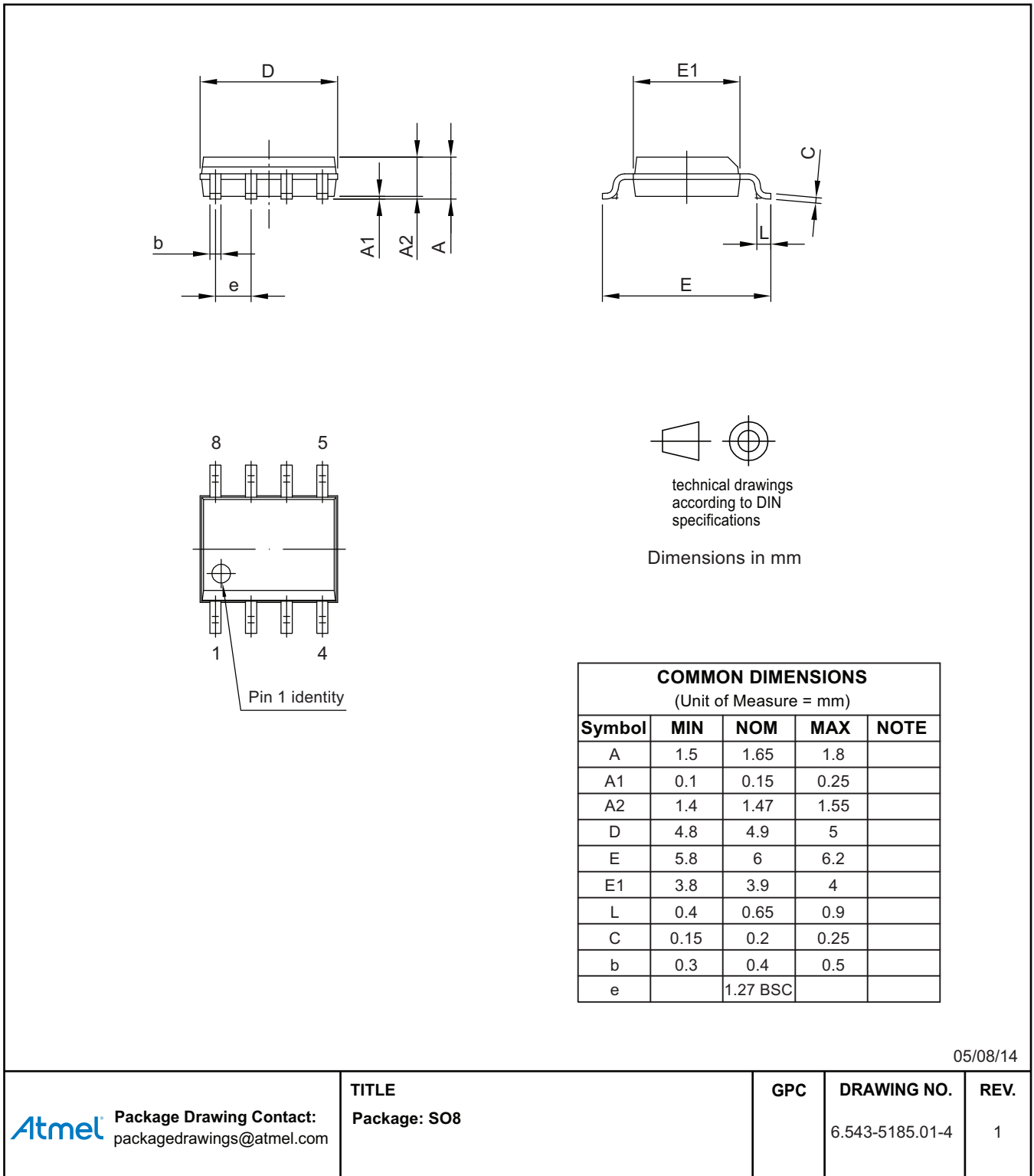
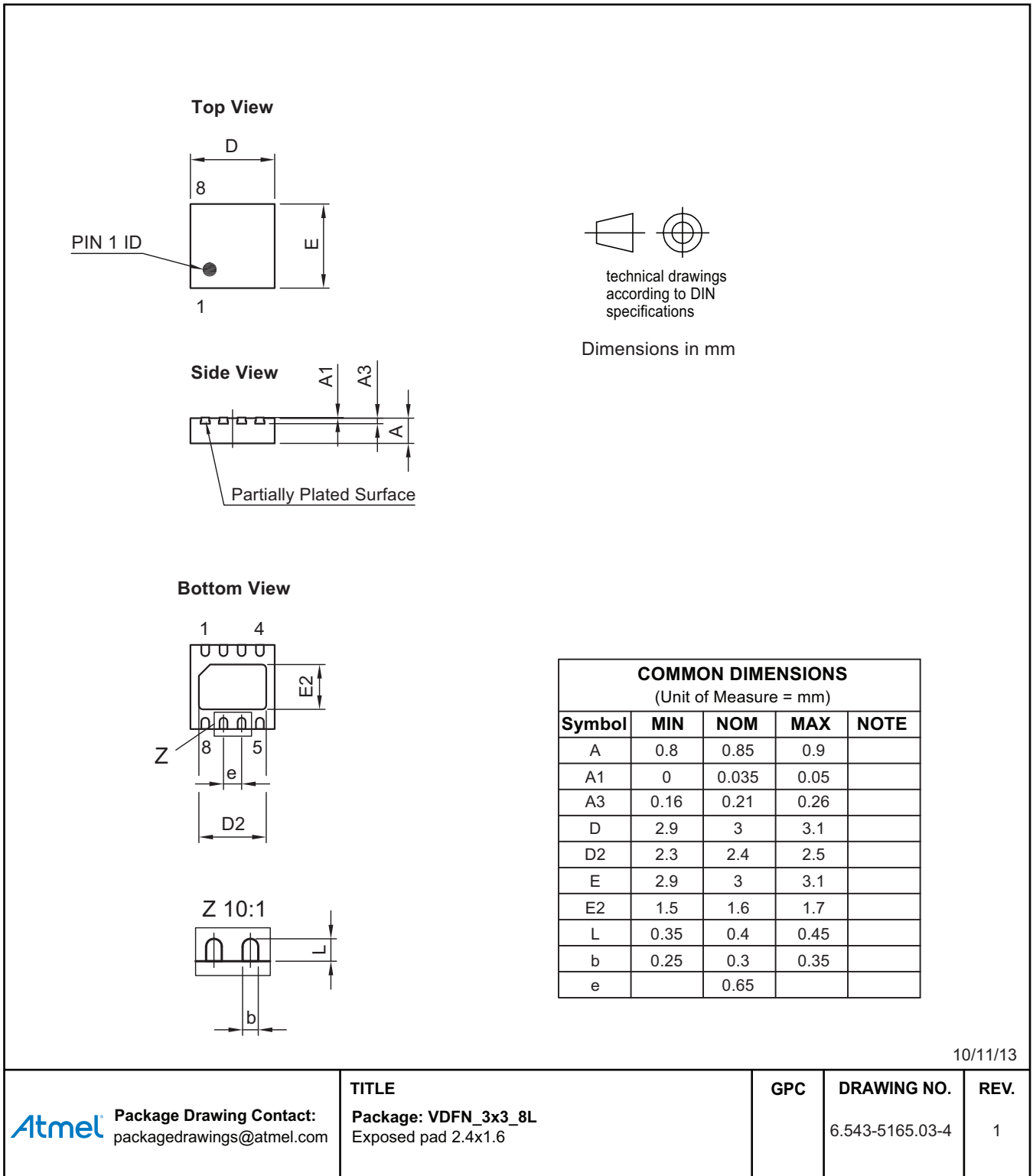


Figure 9-2. DFN8





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